Modeling and Simulation of SAR ADC for Biomedical Applications

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ABSTRACT

This paper presents a 10-bit Successive Approximation Register (SAR) ADC for biomedical applications. Recent technological advances in low-power integrated circuits, with the fastest changing electronics world, the grip which analog electronics has always had, can never be changed or manipulated in any kind of applications. As all the real quantities are analog in nature, in any kind of applications there should be some means to convert those analog quantities into digital logic levels to process the signals according to the applications' requirements. The critical function is converting analog signal to digital signal using analog-to-digital converter (ADC). The binary weighted digital-to-analog converter (DAC) array is considered with total capacitance of 1 pF. The comparator parameter with thermal noise has least significant bit (LSB) of one. There is no comparator offset LSB issue. The SAR logic consider supply voltage of 1-V and resolution of 10-bit with sampling frequency of 1 MS/s. The input signal is at 0.1 MHz with amplitude of 0.45-V and offset of 0.5-V. There is no unit capacitor mismatch is considered. With the unit capacitor mismatch the performance of the ADC degrades. The parametric simulation of thermal noise LSD varies for the ENOB from 8.2 bit to 8.9 bit. The ADC can achieve signal-to-noise-plus distortion of 55 dB and effective number of Bit (ENOB) 8.9 Bits. There is no 2nd term non-linearity and also there is no 3rd term sampling non-linearity.

Keywords: SAR, ADC, Binary weighted DAC, SNR, Biomedical

1. INTRODUCTION

A The analog-to-digital converter (ADC) is a fundamental block in implantable biomedical systems. The successive approximation register (SAR) ADC is very suitable for these applications due to its good power efficiency. Since these systems might be powered with lithium cells or energy harvesting devices, SAR ADCs with low voltage and low power are critically necessary [1]. Ultra-low voltage, which is lower than the sum of the threshold voltage of NMOS and PMOS, brings difficulties to the design of SAR ADCs. Signal swing is limited by the reduction of supply voltage. However, noise does not decrease proportionally. In order to prevent the signal-to-noise ratio (SNR) from decreasing, power consumed by the circuits might be increased. Analog circuits operating under ultralow voltage are still extremely difficult to design. For analog switches, which are widely used in SAR ADCs, have poor conductivity. Conventional one-stage boost circuits cannot generate enough voltage to drive the switches at ultra-low voltage, which leads to serious non-linearity. The power of digital circuits gets sustained benefits from the scaling down of the supply voltage [2]. But ultra-low voltage will lead to heavy leakage current and long logic delay time. Some proposed methods [3]-[4] help to improve the performance of the SAR ADC. However, their control logic circuits are always complicated. At ultra-low voltage, these logic circuits may fail

to work and dissipate much leakage power. So, for low voltage design, simple control logic might be a better choice. A a 10-bit SAR ADC utilized in biomedical applications. To satisfy the system requirements, the supply voltage is reduced to 0.6 V. Theoretical analysis is made to show that conventional bootstrapped switches limit the performance of the SAR ADC. A two-stage bootstrapped sampling switch is designed to enhance the conductivity of the sampling transistor at 0.6-V voltage. As a result, the linearity of the input signal is ensured, and conversion precision is improved. To further simplify the circuit and reduce the power losses, the tail capacitor of the DAC array is reused [5] in the VCM-based switching procedure. Asynchronous control logic is adopted to improve conversion speed, and power dissipation is reduced without using high frequency clock generator. Experimental results show that the designed SAR ADC only consumes 3 μW at the 300-kS/s sampling rate, which is especially suitable for the embedded biomedical-systems. There is an increasing trend in several biomedical applications such as pulse-oximetry, ECG, PCG, EEG, neural recording, temperature sensing, and blood pressure for signals to be sensed in small portable wireless devices. Analog-to-digital converters (ADCs) for such applications only need modest precision (8 bits) and modest speed (40 kHz) but need to be very energy efficient. ADCs for implanted medical devices need micropower operation to run on a small battery for decades. We present a bio-inspired ADC that uses successive integrate-and-fire operations like spiking neurons to perform analog-to-digital conversion on its input current. In a 0.18-m subthreshold CMOS implementation, we were able to achieve 8 bits of differential non-linearity limited precision and 7.4 bits of thermal-noise-limited precision at a 45-kHz sample rate with a total power consumption of 960 nW. This converter's net energy efficiency of 0.12 pJ/quantization level appears to be the best reported so far. The converter is also very area efficient (0.021 mm^2) and can be used in applications that need several converters in parallel. Its algorithm allows easy generalization to higher speed applications through interleaving, to performing polynomial analog computations on its input before digitization, and to direct time-to-digital conversion of event-based cardiac or neural signals [6]. This paper presents SAR ADC design for bio-medical applications. Splitting comparator and energy saving capacitor array are proposed to achieve low power consumption. The average switching energy of the capacitor array can be reduced by 69% compared to a conventional switching method. The measured signal-to-noise-and distortion ratios of the ADC is 58.4 dB at 500KS/s sampling rate with an ultra-low power consumption of 42-μW from a 1-V supply voltage. The ADC is fabricated in a 0.18-μm CMOS technology [7]. This paper describes an ultra-low-power SAR ADC in 0.13-μm CMOS technology for medical implant devices. It utilizes an ultra-low-power design strategy, imposing maximum simplicity in ADC architecture, low transistor count, low-voltage low-leakage circuit techniques, and matched capacitive DAC with a switching scheme which results in full-range sampling without switch bootstrapping and extra reset voltage. Furthermore, a dual-supply scheme allows the SAR logic to operate at 400mV. The ADC has been fabricated in 0.13-μm CMOS. In 1.0-V single-supply mode, the ADC consumes 65nW at a sampling rate of 1kS/s, while in dual-supply mode (1.0V for analog and 0.4V for digital) it consumes 53nW (18% reduction)

and achieves the same ENOB of 9.12. that is the 24% of the 53-nW total power is due to leakage. To the authors' best knowledge, this is the lowest reported power consumption of a 10-bit ADC for such sampling rates [8].

A 10-bit SAR is modeled and simulated. The SAR logic consider supply voltage of 1-V and resolution of 10-bit with sampling frequency of 1 MS/s. The input signal is at 0.1 MHz with amplitude of 0.45-V and offset of 0.5-V. There is no unit capacitor mismatch is considered. With the unit capacitor mismatch the performance of the ADC degrades. The parametric simulation of thermal noise LSD varies for the ENOB from 8.2 bit to 8.9 bit. The ADC can achieve signal-to-noise-plus distortion of 55 dB and effective number of Bit (ENOB) 8.9 Bits. There is no 2nd term non-linearity and also there is no 3rd term sampling non-linearity.

After the introduction, the second section discuss the design of the SAR Design, while the third section describes the modeling and simulation of the SAR ADC. Finally, the section four concludes the paper.

2. SAR ADC DESIGN

A block diagram of this SAR ADC is shown in Figure. 1. It is composed of an inherently matched capacitive DAC, a low-power dynamic latch comparator, a low-leakage/low voltage SAR digital logic, and power-efficient level shifters between the digital logic and the analog blocks. In addition, a differential architecture is employed to have good common-mode noise rejection. A medical implant device, such as pacemakers and implantable cardiac defibrillators, require increasingly advanced signal acquisition and processing systems. Such devices, which are to be implanted in the human body, require extremely low power consumption to operate up to 10 years or more, with a small non-rechargeable battery. SAR ADCs are commonly used in biomedical acquisition systems due to their low power consumption and simplicity, particularly for simple analog sub-circuits. The comparator and sampling switches are the only two analog components. No static power is consumed if preamplifiers are not used. Several power-efficient switching sequences for capacitive digital-to-analog converters (DACs) to reduce the dynamic power consumption. The DAC, as shown in Figure. 2, is implemented with a binary-weighted capacitor array. The unit capacitor in the DAC should be kept as small as possible for power saving. In practice, it is usually determined by the thermal noise and capacitor mismatch. In this design, mismatch is

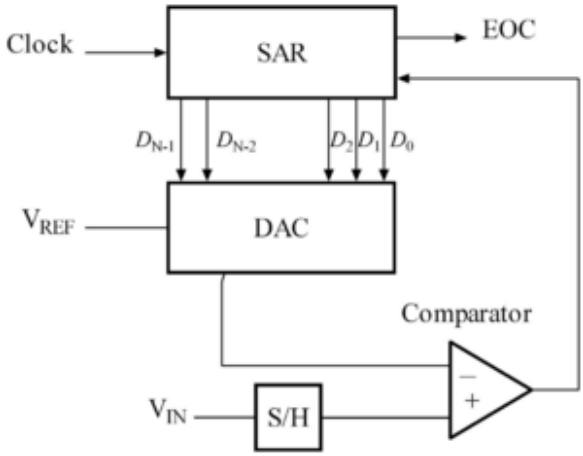

Figure 1: SAR ADC Block diagram

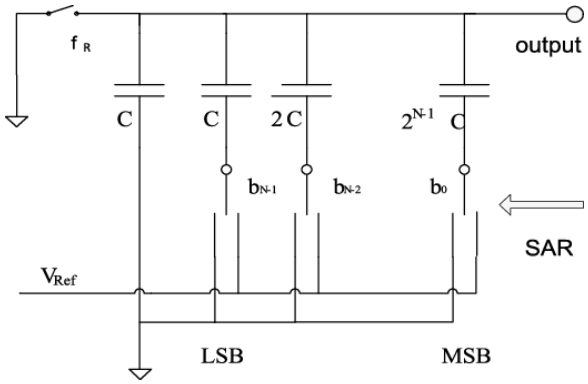

Figure 2: Binary weighted DAC

dominant over thermal noise. Apart from the above limiting factors, the sampling leakage is also a big concern due to the ultra-low speed. A transmission gate is used as the sampling switch at the top plates of the capacitor array. The error voltage introduced by the charge injection is very small as the charge is injected onto the entire array. For a sampling rate as low as 1kS/s, the transistor leakage will introduce significant voltage drop during the hold period. In order to reduce the leakage current, the switch is designed with twice the minimum length and two transistor stacks. The SAR logic is shown in Figure. 1. It generates the sample signal, and the switch control signals for the DAC. The working mechanism of its 10-bit shift resister. A 4-bit counter and a decoder are used to generate the control signals for the 10-bit shift register. The entire logic uses 16 transmission-gate flip-flops, and the decoder has been optimized by hand for minimum logic depth and gate count. The output power spectral density(PSD) of the SAR ADC is shown in Figure 3.

4. CONCLUSION

A 10-bit SAR ADC design for sensor applications. The DAC structures uses split-array capacitive topology. The SAR is modeled and simulated to achieve 8.8-bit resolution. The binary weighted digital-to-analog converter (DAC) array is considered with total capacitance of 1 pF. The comparator parameter with thermal noise has least significant bit (LSB) of one. There is no comparator offset LSB issue. The SAR logic consider supply voltage of 1-V and resolution of 10-bit with sampling frequency of 1 MS/s. The input signal is at 0.1 MHz with amplitude of 0.45-V and offset of 0.5-V. There is no unit capacitor mismatch is considered. With the unit capacitor mismatch the performance of the ADC degrades. The parametric simulation of thermal noise LSD varies for the ENOB from 8.2 bit to 8.9 bit. The ADC can achieve signal-to-noise-plus distortion of 55 dB and effective number of Bit (ENOB) 8.9 Bits. There is no 2nd term non-linearity and also there is no 3rd term sampling non-linearity. t

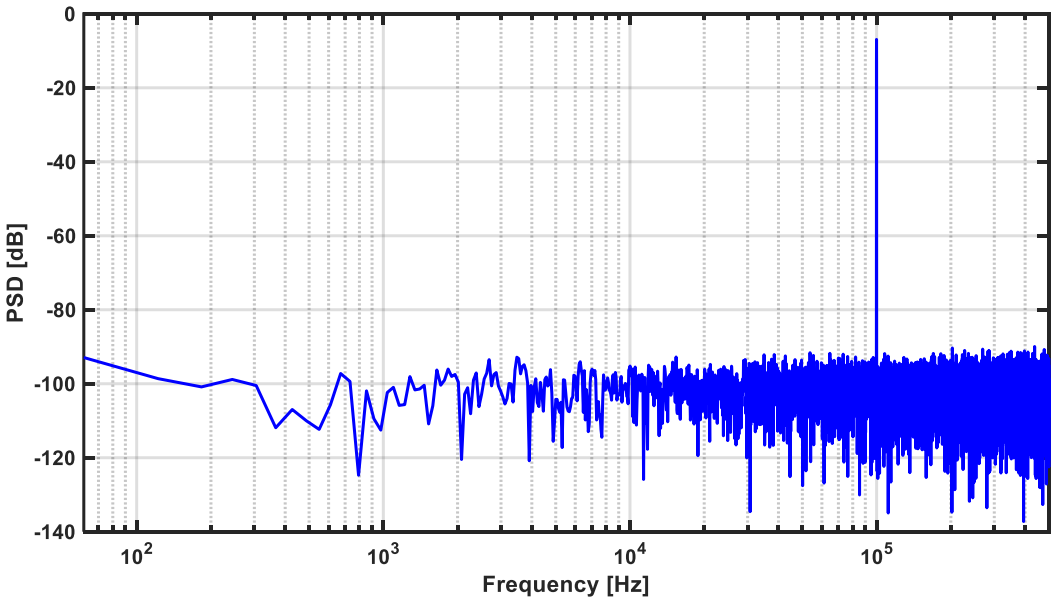

Fig. 3: PSD plot for input signal at 100 kHz

5. ACKNOWLEDGMENT

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